

The SOI-Like Method of Reducing the Die Size of Bulk-Micromachined Sensors

Lung-Jieh Yang and Shung-Wen Kang

Department of Mechanical Engineering, Tamkang University,
No. 151, Yih-Chan Rd., Tamsui, 25137, Taiwan, Republic of China

(Received May 9, 2001; accepted August 31, 2001)

Key words: SOI-like, miniaturization, bulk-micromachining

This paper proposes a new method of miniaturizing bulk-micromachined sensors. A Pyrex glass bonded to a silicon wafer replaces the silicon wafer as a substrate, because the silicon wafer can be machined to a diaphragm afterwards without wasting die area on {111}-faced slopes. Basically, this SOI(silicon-on-insulator)-like method produces sensor dies as small as surface-micromachined ones and is compatible with different techniques of making diaphragms. The silicon diaphragm on a glass substrate is mono-crystalline and has stable mechanical properties and reproducible behavior. The SOI-like method allows the fabrication of piezoresistive pressure sensors with a die size of $1.0\text{ mm} \times 0.8\text{ mm} \times 0.5\text{ mm}$. Finite element analysis and pressure testing are compared to demonstrate the sensor performance of the prototype.

1. Introduction

It is well known that wasting the large die area on {111}-faced slopes prohibits the miniaturization of silicon bulk-micromachined sensors. The enlargement of the die size in silicon bulk-micromachining is due to the propagation of the {111} crystal planes. In silicon, the open window on the opposite side of the wafer is enlarged by a distance of $\sqrt{2}t$, where t is the depth of etching by alkaline solution. A (100) silicon wafer with an etching depth of $500\text{ }\mu\text{m}$ shown in Fig. 1 yields minimum die sizes, larger than the surface features on the front side, of at least $700\text{ }\mu\text{m}$. The die enlargement wastes valuable silicon surface area and imposes a serious limitation on the die count per wafer.⁽¹⁾

On the other hand, the sensing devices fabricated by surface micromachining do not enlarge the die area and promise order-of-magnitude improvements in the dimensions of the die. The consequent reduction in the cost of an individual sensor makes the develop-

Corresponding author, e-mail adress: ljyang@mail.tku.edu.tw

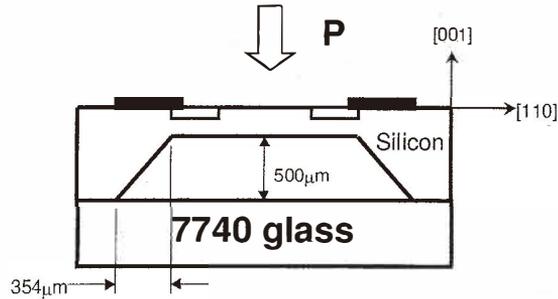


Fig. 1. Classical packaging of micro pressure sensors fabricated by silicon bulk micromachining. The $\{111\}$ -faced slopes around the silicon diaphragm occupy an effective size over $700 \mu\text{m}$ on a 4" wafer with an etching depth of $500 \mu\text{m}$.

ment of microelectronic systems integrated with sensors economically feasible. Whereas typical dimensions for silicon bulk-micromachined sensors are still in the range of several millimeters, surface-micromachined devices are several hundreds of micrometers in size. Additionally, planar processing without corrugated grooves and the on-chip circuitry illustrates the more promising features of surface micromachining technology over bulk micromachining.

2. New Solution to Miniaturizing Sensor Dies

This paper proposes a new strategy for the miniaturization of micro-sensors without the die-enlargement effect of silicon bulk-micromachining.⁽²⁻³⁾ In this strategy, a Pyrex-7740 glass substrate with etched grooves, anodically bonded with a silicon wafer, replaces the bare silicon wafer. The entire silicon wafer with sensing elements attached beforehand, whether piezoresistive or capacitive, can be machined to a thin diaphragm structure without a V-groove configuration on the back surface. This method requires neither double-side photolithography nor anisotropic etching, and no $\{111\}$ -faced grooves are left on the sensor substrate. Figure 2 shows this SOI-like concept.

The new configuration of sensors is somewhat similar to the one made by conventional SOI technology, and is referred to as the "SOI-like" method. The major characteristics of this method are the use of Pyrex glass as the substrate and use of anodic bonding after the fabrication of silicon sensing devices. The glass substrate cannot endure high-temperature processes but has no crucial limitations during wafer bonding. It is particularly useful in solving the sensor miniaturization issue with low-cost processing facilities. Basically, the advantages of this method over silicon bulk-micromachining are similar to the benefits of SOI technology. Therefore, one can design SOI-like sensors as small as the surface-micromachined ones.

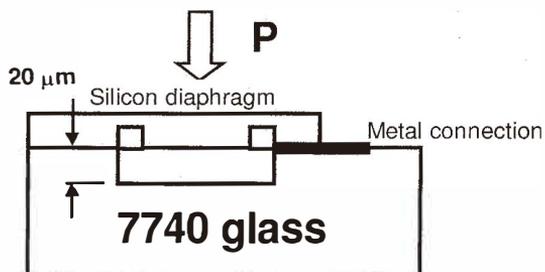


Fig. 2. Cross-sectional view of the SOI-like micro pressure sensor fabricated by silicon bulk-micromachining without the die-enlargement effect.

The other advantages of this method include process compatibility with many bulk-micromachining techniques for making silicon diaphragms. Examples are the time-controlled etching with V-groove depth-rulers,⁽⁴⁾ boron etch-stop,⁽⁵⁾ electrochemical etch-stop,⁽⁶⁾ HNA (hydrofluoric-nitric-acetic acid system) etch-stop,⁽⁷⁾ and even precise lapping/polishing. Moreover, this SOI-like silicon diaphragm is monocrystalline, which means it has well-defined mechanical properties. Compared to the amorphous or polycrystalline thin films of surface-micromachined devices, the crystalline silicon diaphragms provide more stable performance and reproducible characteristics for microsensors.⁽⁸⁾

3. Fabrication Example—Sub-mm Pressure Sensor

Figures 3 and 4 depict the FEM (finite element method) model and the configuration of piezoresistors of a piezoresistive pressure sensor die utilizing the SOI-like structure. The four piezoresistors, which are connected as a Wheatstone bridge circuit, are shown in Fig. 5. Details of the fabrication procedure are shown in Fig. 6 and clarified as follows:

3.1 V-groove etching of alignment keys and depth-rulers

The V-groove depth rulers on a (100) silicon wafer monitor the thickness of the silicon diaphragm with μm resolution. The corresponding circular patterns of oxide masking define the depth of the V-grooves as the diameter of circles because of the self-alignment of crystals in the anisotropic etching solution. This step is economical and useful during the trial-and-error period of R&D. The design of the V-groove array depends on the thickness of the silicon diaphragm.⁽⁴⁾

3.2 Ion implantation for piezoresistors and ohmic-contact area

Ion implantation provides accurate doping concentrations of piezoresistors and ohmic-contact area. A boron dosage of $6 \times 10^{13} \text{ cm}^{-2}$, with the implant energy of 80 KeV, determines the sheet resistance of the piezoresistors in the range of $500 \Omega/\square$. Implantation at a high dosage above 10^{15} cm^{-2} on the ohmic-contact area prevents unknown resistance in the vicinity of the metal contacts.

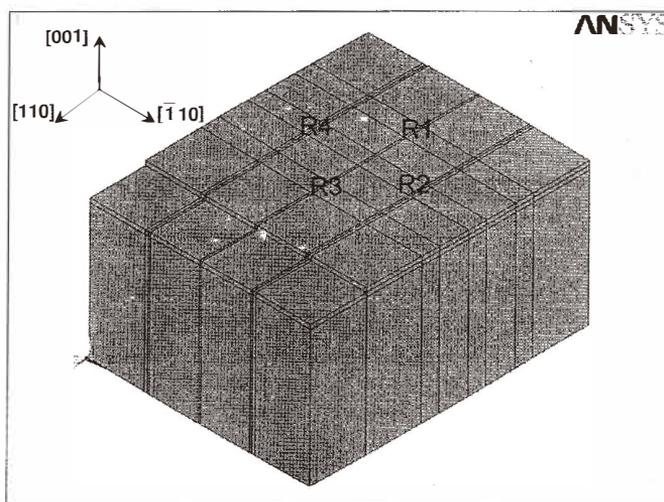


Fig. 3. FEM model of the SOI-like pressure sensor with R_1 ~ R_4 (implanted along $[110]$ direction) denoting the positions of the piezoresistors. The FEM model is composed of three layers including the silicon diaphragm ($400\ \mu\text{m} \times 400\ \mu\text{m} \times 37\ \mu\text{m}$), the glass frame without the cavity portion ($1000\ \mu\text{m} \times 800\ \mu\text{m} \times 20\ \mu\text{m}$), and the glass substrate ($1000\ \mu\text{m} \times 800\ \mu\text{m} \times 500\ \mu\text{m}$), stacked in the vertical $[001]$ direction.

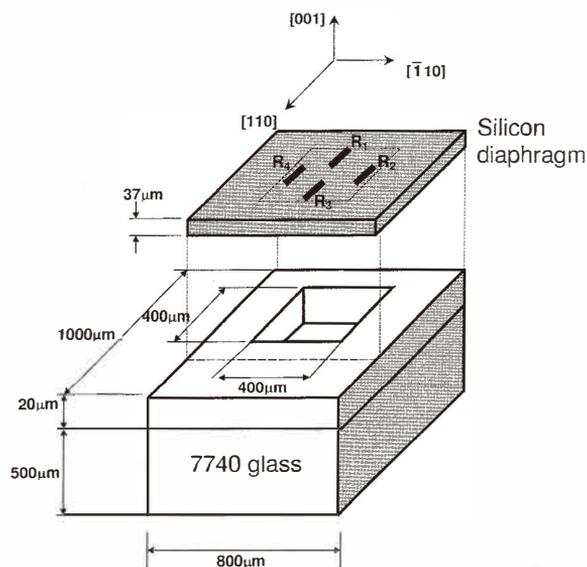


Fig. 4. Arrangement, shape, dimension and crystallographic orientation of the piezoresistors on the diaphragm of the SOI-like structure. R_1 ~ R_4 denote the piezoresistors along the $[110]$ direction, and each has the size of $64\ \mu\text{m} \times 8\ \mu\text{m}$.

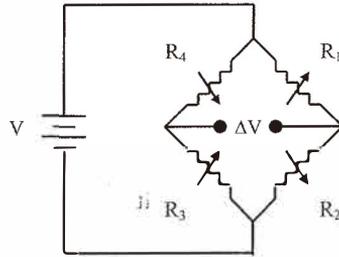


Fig. 5. Wheatstone bridge circuit of a piezoresistive pressure sensor. $R_1 = R_3 = R + \Delta R_1$ and $R_2 = R_4 = R + \Delta R_2$ while pressure is applied to the silicon diaphragm.

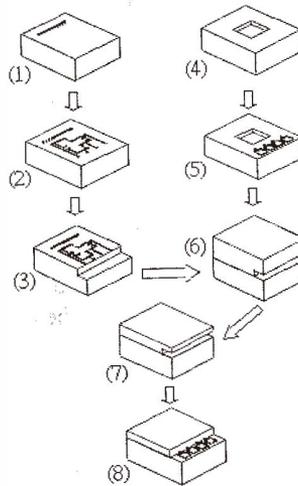


Fig. 6. Fabrication process for the SOI-like pressure sensor.

(1) V-groove etching of alignment keys and depth-rulers, (2) Ion implantation for piezoresistors and ohmic-contact area, (3) Metal evaporation and pad-hole etching, (4) Cavity etching on glass substrate, (5) Metal evaporation on glass substrate, (6) Anodic bonding of silicon and glass substrate, (7) Diaphragm formation, (8) I/O pads opening on glass substrate.

3.3 Metal evaporation and pad-hole etching

The metal evaporated to make the signal connection is aluminum with a thickness of $0.1 \mu\text{m}$. After that, the silicon wafer is protected by photoresist for the etching away of the pad-hole portion, which faces the I/O (input and output) pads on the 7740 glass after wafer bonding. A shallow cavity on the silicon wafer is etched by SF_6/O_2 plasma to a depth of $10 \mu\text{m}$.

Basically, no planar processes occur on the silicon wafer after this step. The following are correlated to the glass substrate and the bonding process.

3.4 *Cavity etching on the glass substrate*

Because the silicon wafer is planar without any cavity grooves for pressure sensors, the pressure cavities must be defined on the Pyrex 7740 glass. This work uses concentrated HF or HNA solutions to etch cavities on glass. The etching mask may be a photoresist with good adhesion or Cr-Au film.⁽⁹⁾ The depth of the pressure cavities depends on the largest deformation of the silicon diaphragm when it is subjected to the maximum pressure loading.

3.5 *Metal evaporation on glass substrate*

The only metal connections that the glass substrate should have are the I/O pads for the piezoresistive signal. Candidates for the metal pads are Cr/Au and Al. To prevent pressure leakage, the metal thickness is generally 0.5–1.0 μm for I/O pads except for the anodic-bonded area below 0.2 μm .

3.6 *Anodic bonding of silicon and glass substrates*

Anodic bonding of silicon and Pyrex 7740 glass is a very popular technique in MEMS. In this study, however, the pre-alignment between silicon and the Pyrex 7740 glass is fairly critical. The accuracy of the alignment primarily determines the location of the piezoresistors with respect to the edge of the pressure cavity and influences the output sensitivity of the sensors.

The bonding temperature should be as far below 500°C as is possible. A temperature too much higher induces residual stress and warps the bonded substrates due to thermal mismatch.

3.7 *Diaphragm formation*

Several techniques can be used to machine the silicon wafer to a thin diaphragm structure. Machining techniques are described in detail in Sec. 5 of this paper.

3.8 *Opening for I/O pads on the glass substrate*

The I/O pads on the glass substrate do not appear after the diaphragm formation process. One additional etching of the silicon diaphragm above the I/O pads is needed. Either metal masking subjected to a TMAH etching solution or photoresist masking subjected to plasma etching completes this step.

The micrograph of the finished micro pressure sensor die is shown in Fig. 7. The die-size after dicing is 1.0 mm \times 0.8 mm \times 0.5 mm.

4. **Remarks on Anodic Bonding**

The oxide layer on the silicon wafer is stripped away before anodic bonding. There are two reasons for this pretreatment. First, it provides good bonding strength between the glass and the silicon without the obstacle of oxide. It is particularly crucial to hermetically seal the pressure sensors. Second, an oxide layer left on silicon cannot prevent a short-circuit between the silicon diaphragm and the metal connections on glass because of high-

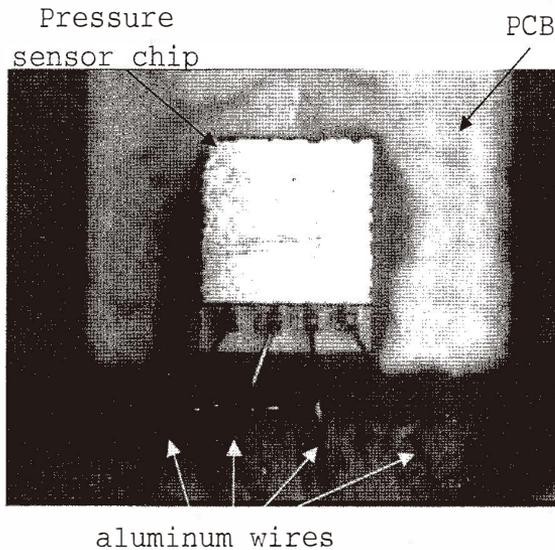


Fig. 7. Optical micrograph of a SOI-like micro pressure sensor after wafer-dicing and wire-bonding. Its dimensions are $1.0\text{ mm} \times 0.8\text{ mm} \times 0.5\text{ mm}$ and the diaphragm has an area of $400\text{ }\mu\text{m} \times 400\text{ }\mu\text{m}$.

voltage breakdown during anodic bonding.

However, electrical isolation is still required between the silicon diaphragm and metal connections on the glass. Designing the pn-junction isolation or burying the layer solves the short-circuit issue. The width of the ohmic-contact routing (e.g., $25\text{ }\mu\text{m}$) must be greater than the width of the metal wire routing (e.g., $15\text{ }\mu\text{m}$). Then the silicon wafer can contact the glass substrate without short circuits among the metal connections because of the p-n junction rectification between p⁺-type and n-type regions.

Although the pre-stripping of the oxide layer on silicon cannot obstruct the anodic bonding, a metal thickness of more than $0.3\text{ }\mu\text{m}$ also prevents good bonding. Particularly to satisfy the strict requirement of no pressure-leakage during sensing, voids due to metal routing along the bonded area are absolutely not permitted.

Compared to the conventional process of silicon bulk-micromachining sensors, the rewards of this SOI-like process more than compensate for the elaborate efforts to reduce the die size of the microsensors.

5. Machining Techniques for Silicon Diaphragms

5.1 Boron etch-stop

To use boron etch-stopping to complete the SOI-like structure, an n-type epitaxial layer is conventionally grown above the p⁺ stop-layer on a p-type silicon wafer. This process has two drawbacks: The EDP etching solution is poisonous, and the nonuniformity in the

thickness is usually greater than 1 μm . This method was not used in the work reported in this paper.

5.2 Electrochemical etch-stop

The n-type epitaxial layer in the electrochemical etch-stop is grown above the p-type substrate. With a negative-biased control during KOH etching, uniformity in thickness of the n-type silicon diaphragm can be achieved very satisfactorily.⁽⁵⁾ After some augmentation of electrical feed-through for the glass-silicon bonded substrate, it will be the most elegant means of making the silicon diaphragm commercially.

5.3 HNA etch-stop

The lightly doped (doping concentration less than 10^{17}cm^{-3}) etch-stop could be achieved by a special HNA isotropic etching solution. The special formulation is HF: HNO_3 : CH_3COOH = 1: 3: 8.⁽⁷⁾ By suitably controlling the concentration of the epitaxial n-layer above the highly conductive p-substrate (resistivity $< 0.01 \Omega\text{-cm}$), the HNA solution nearly stops on the epitaxial interface without any etching-protector or electrical connection around the silicon diaphragm. This method seems to be the simplest means of batch-fabrication, if the surface roughness and the etching selectivity are to be guaranteed.

5.4 Precise lapping/polishing

Because there are no {111}-planes to define the sensor pattern, it is not necessary to obtain the silicon diaphragm by anisotropic silicon etching. Mechanical lapping/polishing is useful as well. The prototype of the SOI-like pressure sensors described in Sec. 7 is fabricated easily in this way.

6. Price Niche for the SOI-like Pressure Sensor

The electronic tire pressure gauge with digital display for cars, shown in Fig. 8, is a popular MEMS product available on the consumer-electronics market. The need for low-price and multiple functions in such a product requires lower cost semiconductor pressure sensors.

By SOI-like technology, as described in this paper, the cost of each sensor die can be brought down to US\$ 0.20 or even lower by improvements in the miniaturization of die size and sensor density on each wafer. In the current fabrication technique, the dicing trail on a glass substrate wider than 100 μm limits the smallest die size for the SOI-like sensors. Therefore, the smaller die size and the lower price of the pressure sensor are promising after modification of the process.

7. Pressure Testing and Discussion of Results

The pressure sensor shown in Fig. 7, with a silicon diaphragm 37 μm thick made using the LAPMASTER-5 lap/polish machine, was tested in a standardized testline (Taiwan Silicon Microelectronic Corporation, Kaoshiung, Taiwan) over a pressure range from 0 to 100 psi. A classical set of output-voltages is shown in Fig. 9. The sensitivity (slope) of the

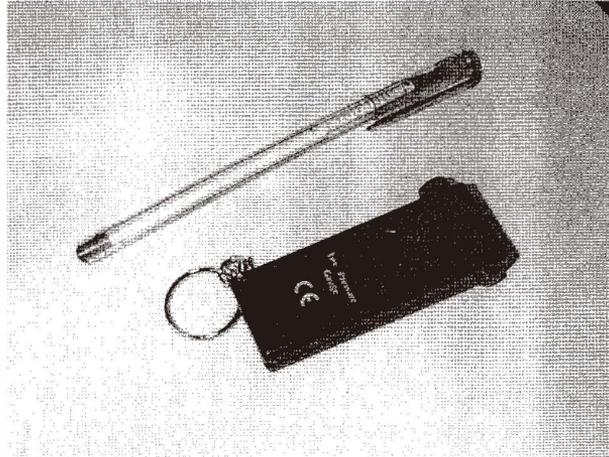


Fig. 8. Electronic tire-pressure gauge with digital display for cars (Taiwan Silicon Microelectronic Corporation, Kaoshiung, Taiwan).

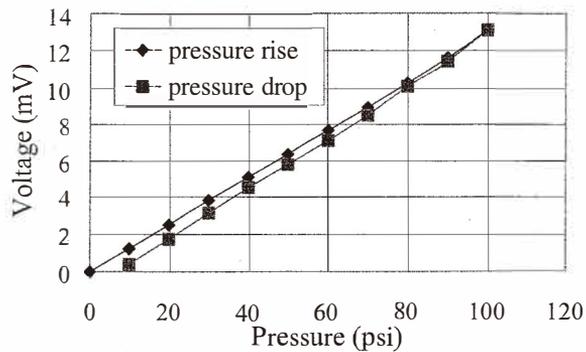


Fig. 9. A classical set of output-voltages (with dropping of the offset voltage) from the SOI-like pressure sensor. The bias voltage for the Wheatstone bridge of piezoresistive sensors is 3 V. The output data are summarized in Table 2.

voltage-vs-pressure curve deviates within 10% over 3 months, and no pressure leakage from the glass chamber is observed.

We also calculated the numerical output voltage of the piezoresistive pressure sensor using ANSYS 5.3 FEM software, and manipulated the stress output as strictly as possible. First, FEM predicts the stress distribution based on the mesh depicted in Fig. 3, using isotropic solid element 45 and anisotropic solid element 64. The sensor dimensions and

properties of materials are listed in Table 1. Then the stress components $\sigma_x^{1,2}$ and $\sigma_z^{1,2}$ of the output of the solid elements corresponding to piezoresistors are extracted manually and converted into the resistance changes $\Delta R_{1,2}$ as well as the voltage output ΔV of the Wheatstone bridge depicted in Fig. 5 by the formula for the piezoresistivity effect shown below:

$$\frac{\Delta V}{V} = \frac{R_3}{R_3 + R_4} \frac{R_2}{R_1 + R_2} = \frac{\Delta R_1 - \Delta R_2}{2R + (\Delta R_1 + \Delta R_2)} \quad (1)$$

$$\frac{\Delta R_{1,2}}{R} = \sigma_z^{1,2} \Pi_1 + \sigma_x^{1,2} \Pi_1, \quad (2)$$

where R is the resistance before pressure loading and V is the bias voltage of the Wheatstone bridge. The absolute values of stress components σ_x and σ_z are not identical for the piezoresistors R_1 and R_2 in general. Then the term $(\Delta R_1 + \Delta R_2)$, proportional to the pressure load under the assumption of small deformation, does not vanish in (1). This indicates the slightly nonlinear behavior of the output voltage of the diaphragm-type piezoresistive pressure sensor. The longitudinal and lateral piezoresistive coefficients Π_1 , and Π_l in (2), are

$$\begin{aligned} \Pi_1 &= \frac{1}{2}(\Pi_{11} + \Pi_{12} + \Pi_{44}) \\ \Pi_l &= \frac{1}{2}(\Pi_{11} + \Pi_{12} - \Pi_{44}). \end{aligned} \quad (3)$$

Table 1
Sensor dimensions and properties of materials.

Sensor Description	Dimension or properties
Total die size	1000 μm \times 800 μm (area) \times 500 μm (thickness)
Diaphragm size	400 μm \times 400 μm (area) \times 37 μm (thickness)
Diaphragm material	n-type, (100) single-crystalline silicon with $\rho = 1-10 \Omega\text{-cm}$
Substrate	Pyrex 7740 glass
Piezoresistor	p-type single-crystalline silicon with sheet resistance of $\rho/t = 500 \Omega/\square$
Piezoresistive coefficient, $\Pi_{11}^{(10)}$	6.6×10^{-11} Pa (p-type, $\rho = 7.8 \Omega\text{-cm}$)
Piezoresistive coefficient, $\Pi_{12}^{(10)}$	-1.1×10^{-11} Pa (p-type, $\rho = 7.8 \Omega\text{-cm}$)
Piezoresistive coefficient, $\Pi_{44}^{(10)}$	138.1×10^{-11} Pa (p-type, $\rho = 7.8 \Omega\text{-cm}$)
Young's modulus of isotropic silicon ⁽¹¹⁾	168 GPa
Shear modulus of isotropic silicon ⁽¹¹⁾	61.6 GPa
Elastic constant of silicon, $C_{11}^{(11)}$	164.8 GPa
Elastic constant of silicon, $C_{12}^{(11)}$	63.5 GPa
Elastic constant of silicon, $C_{44}^{(11)}$	79 GPa
Young's modulus of isotropic 7740 glass	60 GPa
Poisson's ratio of isotropic 7740 glass	0.2

Table 1 depicts the numerical values of Π_{11} , Π_{12} and Π_{44} shown in (3).⁽¹⁰⁾

The concordance output data including sensitivity, linearity and hysteresis are summarized in Table 2. The measured sensitivity deviates from the FEM expectation within 25%. Such a degradation of sensitivity may be primarily due to the misalignment errors of the silicon piezoresistors before anodic bonding. The measured linearity also surpasses the commercial specification of 1% by a slight amount.

The comparison in Table 2 also shows that the overestimated sensitivity of the piezoresistive pressure sensor with applying the isotropic postulate of the silicon diaphragm is not crucial. This observation is not as apparent as indicated in the conclusion of ref. (11). The reason clarified here is that the comparative index in this case is the planar stress but not the vertical deformation of the silicon diaphragm. Despite this, the fact that the sensitivity predicted by anisotropic FEM comes closer to the result of testing than to the isotropic result in this case of an SOI-like pressure sensor still concurs with the argument mentioned in ref. (11).

Because of the technical constraints of lapping, the process described in this paper fabricates the SOI-like pressure sensor with a silicon diaphragm no less than 37 μm thick. Higher sensitivity is reasonably expected from 0.04 mV/V/psi up to 0.15 mV/V/psi, if the diaphragm thickness can be reduced below 20 μm by electrochemical etch-stop.

8. Other Potential Applications of SOI-Like Diaphragm Structures

The SOI-like technology can not only fabricate sub-mm pressure sensors, but can also prepare diaphragm structures on glass substrates with cavities beforehand. One additional RIE process can easily define the contours of levitated microstructures, *e.g.*, the comb structures of band-pass resonators⁽¹²⁾ or mass-tether vibrators of accelerometers,⁽¹³⁾ from the original silicon diaphragms. No problem of surface stiction exists for the levitated structures because no sacrificial layers underneath need to be removed. Moreover, some high-aspect-ratio structures can be made from this SOI-like substrate for the easy preparation of silicon diaphragms thicker than 20 μm .

9. Conclusions

This paper describes the new SOI-like method for miniaturizing piezoresistive pressure sensors down to sub-mm size. This method provides an enormous increase in the sensor density per wafer and enables a much lower price for sensors, thus making it possible for

Table 2
Output data of the SOI-like pressure sensor.

(diaphragm size; 400 $\mu\text{m} \times 400 \mu\text{m} \times 37 \mu\text{m}$)			
Data source	Sensitivity (mV/V/psi)	Linearity (%)	Hysteresis (%)
Isotropic FEM (ANSYS solid 45)	0.0546	0.23	Not available
Anisotropic FEM (ANSYS solid 64)	0.0542	0.22	Not available
Pressure testing (Fig. 9)	0.0436	1.48	6.49

them to compete with the products of surface micromachining technology in commercial markets. Comparing the testing results with those of the FEM simulation shows that this much smaller pressure sensor, fabricated in the noncommercial laboratory, has an output sensitivity 25% less than the numerical estimation. In addition to the pressure sensors, some emerging applications of single-crystalline silicon microstructures can be developed by using this SOI-like technology.

Acknowledgment

This work is financially supported by the National Science Council, Taiwan (Republic of China) under project number NSC-89-2218-E-032-002. The authors acknowledge with appreciation the help from Taiwan Silicon Microelectronic Corporation, Kaoshiung, Taiwan.

References

- 1 S. M. Sze: *Semiconductor Sensors* (Wiley, 1994) p.55.
- 2 L.-J. Yang, C.-J. Chang, and Y.-M. Chang: *Proc. Sensor* **99** (1999) p. 397.
- 3 L.-J. Yang and Y.-M. Chang: Taiwan patent 390962 (2000).
- 4 P.-Z. Chang and L.-J. Yang: *J. Micromech. Microeng.* **8** (1998) 182.
- 5 A. Bohg: *J. Electrochem. Soc.* **118** (1971) 401.
- 6 T. N. Jackson, M. A. Tischler, and K. D. Wise: *IEEE Electron. Device Letter*, **EDL-2** (1981) 44.
- 7 W. Goepel: *Sensors - A Comprehensive Survey: Volume 7 Mechanical Sensor*, VCH, Chapters 5 and 14 (1994).
- 8 S. M. Sze: *Semiconductor Sensors* (Wiley, 1994) p. 56.
- 9 S. Shoh and M. Esashi: *Technical Digestion of the 9th Sensor Symposium* (1990) p. 27.
- 10 S. M. Sze: *Semiconductor Sensors* (Wiley, 1994) chapter 5.
- 11 G. S. Chen, M. S. Ju and Y. K. Fang: *Sensors and Actuators A* **86** (2000)108.
- 12 L.-J. Yang, T.-W. Huang and P.-Z. Chang: *Sensors and Actuators A* **90** (2001) 148.
- 13 W. Kuchnel and S. Sherman: *Sensors and Actuators A* **45** (1994) 7.