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Linear Variable Differential Transformer Signal Conditioning Circuit Based on Phase-Locked Loop

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The purpose of this paper is to propose a novel technique for extracting the position signal from an inductive displacement transducer named a linear variable differential transformer (LVDT). In general, the movement of the LVDT core causes its primary inductance change in linear form. The primary winding of the LVDT is used as a time-dependent element for the triangular and square wave generator, which can be called self-oscillation, to generate frequency. The advantage of the proposed technique is that it can measure the displacement using the LVDT without an external oscillator. The change in primary inductance causes the frequency deviation generated by the oscillator. The deviated frequency is captured and converted into a voltage signal using the principle of the phase-locked loop. All the components used in this study are commercially available. The merits of this proposed technique are simple configuration, small size, and low cost. Moreover, the operating range of the LVDT can be extended without the limitation of the nonlinear transfer characteristic. The performance of the proposed technique is discussed in detail and confirmed by experimental implementation. Experimental results show that the maximum error from the proposed technique is about 0.42% and the operating range of the LVDT can be extended to more than 200%. It can be seen that the proposed technique is suitable for embedded measurement in small or micro robots.

1. Introduction

A displacement sensor is one of the important transducers provided for robotics and autonomous machines. Usually, the displacement sensor is used for position determination and is also known as a term position sensor. A linear variable differential transformer (LVDT) is the most famous sensor for accurate measurement. This is due to its high accuracy, high resolution, and robustness.[1–5] One disadvantage of the LVDT is its huge structure compared with its linear operating range. Owing to its huge structure, further reduction in the size of small or micro robots is probably impossible or complicated. The LVDT is usually provided for the measurement of displacement, position, level, flow, force, and pressure. Many applications of the LVDT are

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included in the fields of engineering, industry, military, robotics, agriculture, and scientific and medical equipment.[1–15] The LVDT structure consists of a primary winding, two secondary windings, and a moving core. The operation of the LVDT is the same as that of a conventional transformer, where two secondary windings are series-opposite-connected.[1–3] The resulting signal from two secondary windings is in the form of an amplitude modulation with suppressed carrier (AMSC).[16] Therefore, a synchronous demodulator is required to extract the position signal from the AMSC signal. There are many synchronous demodulators previously proposed.[16–19] However, the small synchronous demodulator proposed in the literature[16] is suitable for embedding in small or micro robots. The behavior of the LVDT provides a narrow linear operating range. Normally, the linear operating range of the commercial LVDT is about 10 to 20% of its structure. Therefore, the measurement of long displacement will require a large structure of the LVDT, which results in a large overall system. Recently, there have been many techniques used to extend the linear operating range without changing the LVDT structure.[20–24] The techniques for extending the linear operating range of the LVDT based on the fractional order and artificial neural network (ANN) have been proposed in the literature.[22,24] However, both techniques require a high-speed signal processing unit. Another disadvantage of these techniques is that the response time is long. Circuit techniques for extending the linear operating range have been proposed.[18–20] The use of the circuit technique to extend the operating range has the advantage in terms of short response time. However, the techniques for extending the linear range require many active components, which cause a large circuit configuration. In addition, an external oscillator is required to excite the LVDT for all the LVDT signal conditioner schemes. It can be seen that the techniques mentioned above are unsuitable for the embedded measurement system and economical attention.

In this paper, a novel technique for the LVDT signal conditioner scheme is proposed. The proposed technique provides the LVDT as a time-dependent device to generate triangular and square waves, called self-oscillation. Therefore, the proposed technique without an external oscillator is obtained. The primary winding of the LVDT is used for self-oscillation. The position movement of the LVDT core causes a linear change in the inductance of the primary winding. Also, the linear variation in the inductance of the primary winding occurs throughout the full stroke range of the LVDT structure. Moreover, the principle of a phase-locked loop (PLL) is used to extract the position instead of the synchronous demodulator. Therefore, the proposed technique provides the advantages of extended operating range, small size, and the absence of an external oscillator, which is suitable for small or micro robots and autonomous machines.

2. Principle

The proposed technique can be separated into three parts, namely, LVDT, triangular and square generator, and PLL. The principle of each part can be explained as follows.

2.1 LVDT

The principle of the LVDT is based on the concept of a conventional transformer, which consists of a primary winding W_P and two identical secondary windings W_{S1} and W_S, and a one-

dimensional moving core, as shown in Fig. 1(a).[17,18,20] The two secondary windings are connected in series with opposite directions. The equivalent circuit of the LVDT is shown in Fig. 1(b). If the excitation signal v_p is applied to the primary winding W_P and the moving core is varied to the position l, the resulting signal $v_s = (v_{s1} - v_{s2})$ can be expressed as [17,18,20]

$$v_s = k_t \left(1 - k_n l\right) l, \tag{1}$$

where k_t and k_n denote the sensitivity and nonlinear coefficient, respectively. Note that the signal v_s is in the form of the AMSC. Therefore, a synchronous demodulator is required to extract the position signal v_{ps} from the signal v_s as shown in Fig. 1(b). The plot of the signal v_{ps} versus the position l of the moving core is shown in Fig. 1(c). From Eq. (1) and Fig. 1(c), it can be seen that the signal v_{ps} is nonlinear over the entire stroke range of the LVDT.

From Eq. (1), the signal v_s is in the form of a transfer characteristic of the LVDT. If the inductance of the primary winding is considered instead of the voltage signal at the primary and secondary windings, then the primary-winding inductance is proportional to the position of the moving core. In this consideration, the secondary winding of the LVDT is terminated by the high resistance as shown in Fig. 2(a). The inductance L_p considered from the primary winding side is dependent on the position l of the moving core. The movement of the moving core causes the change in the primary-winding inductance ΔL. The structure of the LVDT for the consideration of the inductance for the primary winding side is shown in Fig. 2(b). If the moving core moved in the rod of the primary winding, then the inductance of the primary winding can be given by[3]

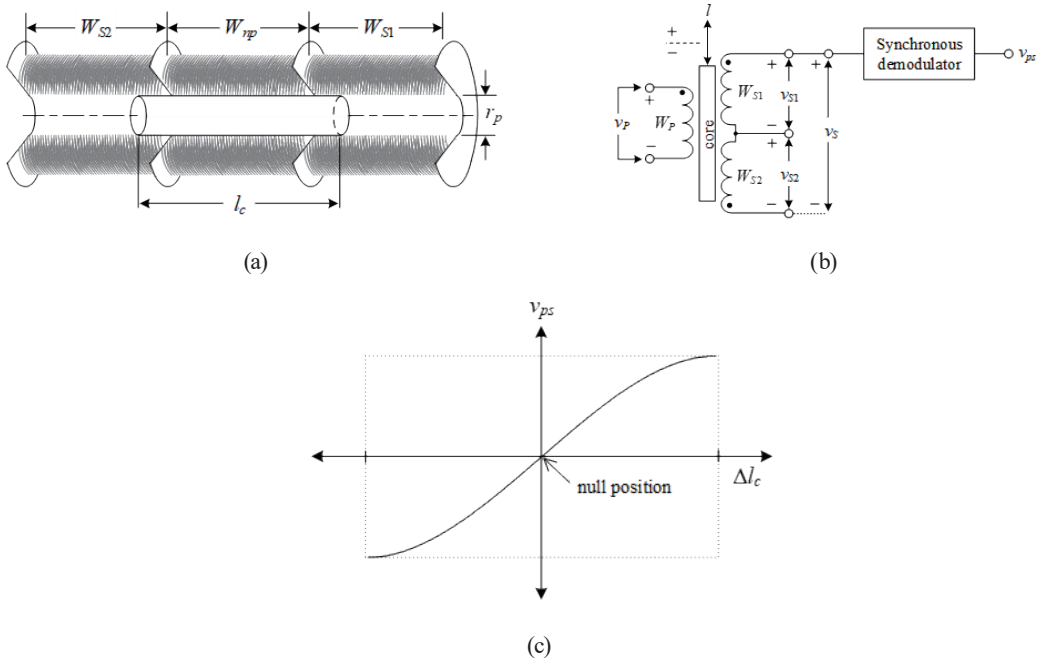


Fig. 1. (a) Structure of LVDT, (b) equivalent circuit, and (c) transfer characteristic.

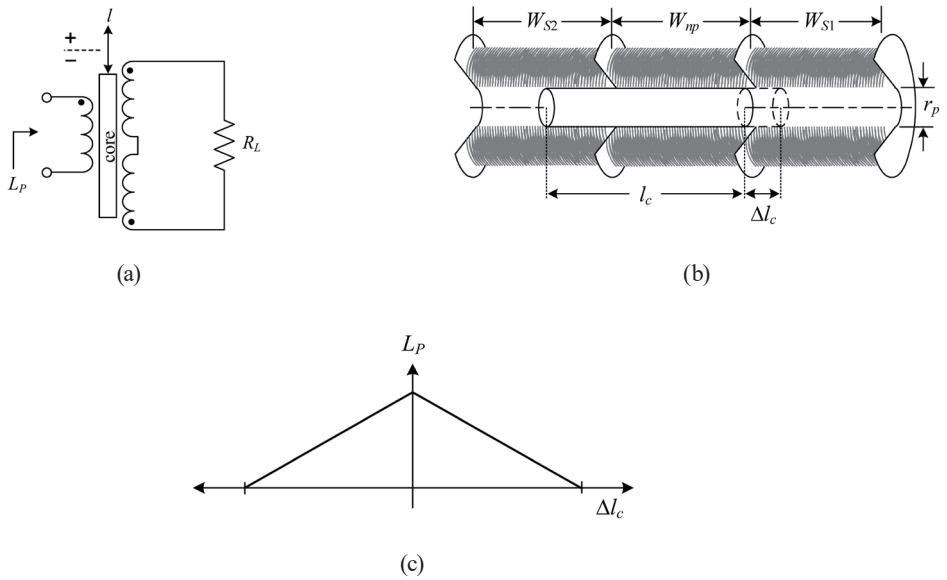


Fig. 2. (a) Equivalent circuit, (b) structure for inductance consideration, and (c) characteristic.

$$L_p + \Delta L = \frac{4\pi^2 n_p^2 \left[W_{np} r_p^2 + \left(\mu_p - 1 \right) r_c^2 \left(l_c + \Delta l_c \right) \right]}{10^7 W_{np}^2} = K_1 K_2 + K_1 K_3 \left(l_c + \Delta l_c \right), \tag{2}$$

where n_p is the number of turns for the primary winding, r_c is the radius of the moving core, μ_p is the permeability of the moving core, l_c is the length of the moving core, and W_{np} is the length of the primary winding. From Eq. (2), the change in the primary-winding inductance ΔL can be stated as

$$\Delta L = \frac{4\pi^2 n_p r_c^2 \left(\mu_p - 1 \right) \Delta l_c}{10^7 W_{np}^2} = K_1 K_3 \Delta l_c . \tag{3}$$

Figure 2(c) shows the plot of the inductance L of the LVDT versus the position of the moving core. It can be seen that the inductance change ΔL is linearly proportional to the position change Δl_c of the moving core.

2.2 Triangular and square wave generator

To achieve the inductance of the primary winding, the triangular and square wave generator (TSWG) is provided in this paper. The TSWG circuit diagram is shown in Fig. 3(a). From the circuit in Fig. 3(a), an operational amplifier (opamp) A_1, the primary winding of the LVDT, and the resistor R_{tr} form an integrator to provide the signal v_{tr} in the triangular form. The triangular signal v_{tr} is converted to a square wave signal v_{sq} by the window comparator formed by opamp A_2 and the resistors R_1 and R_2. The zener diodes D_{Z1} and D_{Z2} provide the zener voltage equal to

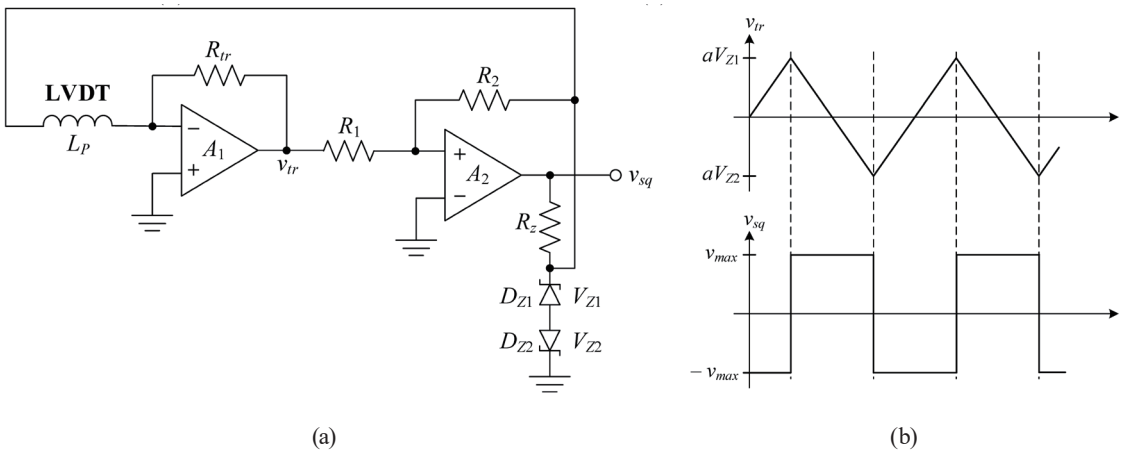


Fig. 3. (a) Triangular and square wave generator, and (b) signals of v_{tr} and v_{sq}.

V_Z. The threshold voltages of the window comparator, v_{thp} and v_{thn}, are equal to aV_Z and $-aV_Z$, respectively, and $a = R_1/R_2$. The output signal v_{sq} is limited by the zener diodes D_{Z1} and D_{Z2} and the resistor R_Z to maintain the maximum voltage of the voltage signal v_L equal to the threshold voltages v_{thp} and v_{thn}. The voltage signal v_L is fed back to the LVDT to generate the triangular signal as shown in Fig. 3(b). From the routine circuit analysis, the frequency f_o of the voltage signal v_{sq} can be expressed as

$$f_o = \frac{R_{tr}V_Z}{4a\left(V_Z + V_D\right)\left(L_p + \Delta L\right)} = \frac{R_{tr}V_Z}{4L_p a\left(V_Z + V_D\right)\left(1 + \dfrac{\Delta L}{L_p}\right)}, \tag{4}$$

where $V_D = 0.7$ V is the voltage across the zener diode in a forward bias state.

2.3 PLL

A block diagram of the PLL is shown in Fig. 4(a).[25] The PLL used in this study is a commercially available device. A phase detector (PD) is used to detect the phase and the difference between the frequencies f_{in} and f_{out}. A low-pass filter (LPF) is provided to cancel the high frequency from the PD. The output signal v_{LF} of the LPF is sent to the input of the voltage-controlled oscillator (VCO) to generate the square wave signal. The behavior of the VCO is shown in Fig. 4(b). The VCO will generate the frequency range from the lower frequency f_L to the upper frequency f_H, and the center frequency f_0 is usually set as the middle of the frequency range. The output signal v_{LF} is the output from the LPF and also the resulting signal from the difference signal between the frequencies f_{in} and f_{out}. Therefore, the operation of the PLL is that the output frequency f_{out} of the VCO will follow the input frequency f_{in}. The output frequency of the PLL is equal to the center frequency f_0 for the null input frequency. In this case, the input voltage signal of the VCO or the output voltage v_{LF} from the LPF is assigned to half of the power supply of the PLL. If the difference between the input frequency f_{in} and the output frequency

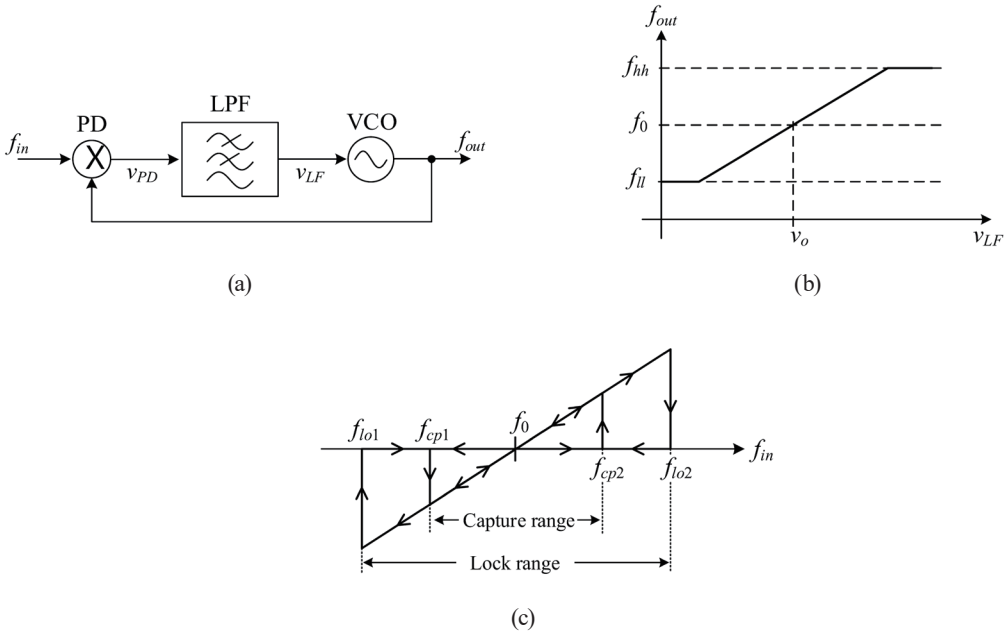


Fig. 4. (a) Block diagram of PLL, (b) VCO behavior, and (c) transfer characteristic of PLL.

f_{out}, $(f_0 - f_{in})$ is in the pass band of the LPF, then the VCO will capture and generate the output frequency f_{out} to follow the input frequency. Also, if the difference frequency is higher than the cutoff frequency of the LPF, then the output frequency f_{out} is back to the center frequency f_0. Similarly, if the input frequency f_{in} is varied from high to low, then the PLL starts to capture and generate the output frequency f_{out} to follow the input frequency f_{in} for the difference frequency $(f_0 - f_{in})$ within the pass band of the LPF. The transfer characteristic of the PLL is shown in Fig. 4(c). From Fig. 4(c), the ranges of the frequencies f_{cp1} to f_{cp2} and f_{lo1} to f_{lo2} are called capture and lock ranges, respectively. For the derivation of the input frequency f_{in}, the PLL will generate the output frequency f_{out} to follow the input signal. Simultaneously, the input signal v_{LF} of the VCO will vary according to the change in the input frequency f_{in}. Note that the PLL can be provided as a demodulator for frequency modulation (FM).

3. Proposed Technique for LVDT Signal Conditioning

The LVDT signal conditioning proposed in this paper is based on the self-oscillation of the LVDT to provide the change in the frequency generated by the TSWG. This change in frequency is similar to the FM form. Therefore, the position of the moving core can be extracted from the FM signal mentioned above.

3.1 Circuit description

The simplified circuit of the proposed technique is depicted in Fig. 5(a). The LVDT is on the left of Fig. 5, where the secondary winding is terminated by the resistance of 100 kΩ. The PLL

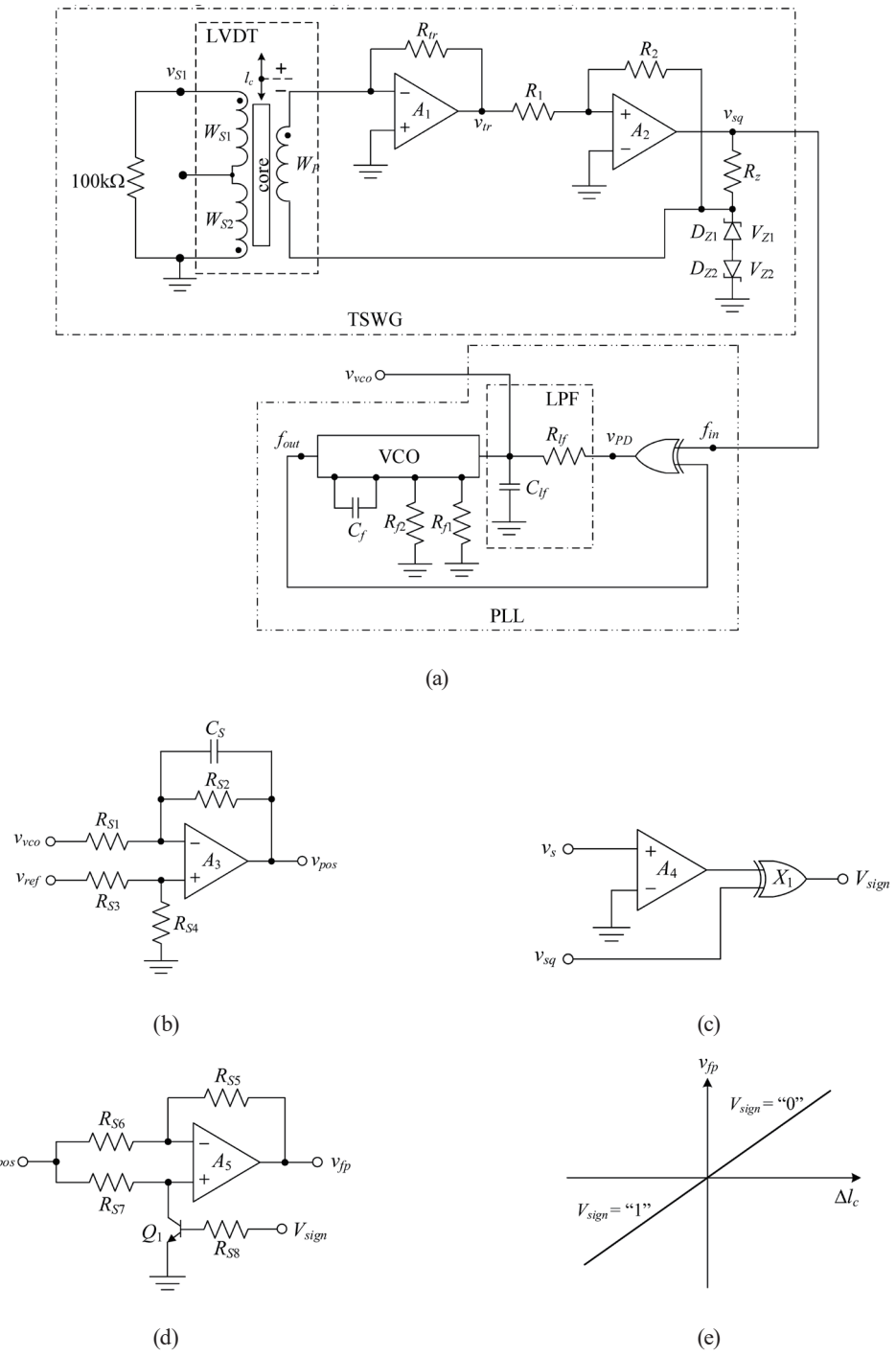


Fig. 5. (a) Proposed circuit, (b) summing amplifier, (c) phase investigator, (d) phase-controlled amplifier, and (e) PCA behavior.

used in this study is the commercially available device in integrated circuit form (CD4046). The phase detector of the commercial PLL is an exclusive OR gate (XOR). The operation of the proposed circuit can be explained as follows. The primary winding W_p of the LVDT and the

active elements, namely, opamps A_1 and A_2, and zener diodes D_{Z1} and $D_{Z2,}$ function as the TSWG. The zener voltages of D_{Z1} and D_{Z2} are assigned as V_Z. The change in the position of the moving core causes the inductance of the primary winding to change. Therefore, the frequency of the output signal v_{sq} also deviates. The signal v_{sq} is transferred to the input of the PLL as the input frequency f_{in}. The difference between the input frequency f_{in} and the output frequency f_{out} is determined by the XOR phase detector. The output signal v_{PD} of the PD is filtered by the LPF formed by the resistor R_{lf} and the capacitor C_{lf} as the signal v_{vco}. The signal v_{vco} forces the VCO to generate the output frequency f_{out} to lock with the input frequency f_{in}. At the same time, the signal v_{vco} also exhibits a magnitude inversely proportional to the change in the inductance of the primary winding. From Eqs. (2) and (4), the output frequency f_{out} and the deviation of the output frequency, Δf, can be stated as

$$f_{out} + \Delta f = \frac{K_f}{\left(1 + \dfrac{K_3 \Delta l_c}{\left(K_2 + K_3 l_c\right)}\right)} = \frac{K_f}{\left(1 + K_c \Delta l_c\right)}, \tag{5}$$

where $K_f = \dfrac{R_{tr} V_Z}{4 a L_P K_1 \left(V_Z + 2V_D\right)}$.

From Eq. (5), the output frequency $f_{out} + \Delta f$ is inversely proportional to the change in the position of the moving core, Δl_c. Note that the term K_3 in Eq. (2) is very small compared with the term K_2, which causes the term K_c to be small. If the change in the inductance of the primary winding causes the TSWG to generate the frequency in a narrow range, the output frequency range of the PLL is also narrow. On the basis of the binomial series, Eq. (5) can be expressed as[26]

$$f_{out} + \Delta f = K_f \left[1 - K_c \Delta l_c + \left(K_c \Delta l_c\right)^2 - \left(K_c \Delta l_c\right)^3 + \ldots\right]. \tag{6}$$

The second-order and higher-order terms in the square brackets on the right of Eq. (6) are very small and can be neglected. Therefore, Eq. (6) can be approximated as

$$f_{out} + \Delta f = K_f \left(1 - K_c \Delta l_c\right) = K_f \left[1 - \frac{K_3 \Delta l_c}{\left(K_2 + K_3 l_c\right)}\right]. \tag{7}$$

From Eq. (6), if the moving core is moved farther into the LVDT, then the inductance of the primary winding increases and the deviation of the output frequency Δf can be given by

$$\Delta f = -K_f K_c \Delta l_c = -\frac{K_f K_3 \Delta l_c}{\left(K_2 + K_3 l_c\right)}. \tag{8}$$

It can be seen that the deviation frequency Δf decreases if the position Δl_c is increased. The conversion gain of the VCO is assigned as K_{vco} in kHz/V. The conversion gain K_{vco} can be determined from the frequency range between the highest and lowest frequencies and the input voltage of the VCO as

$$K_{vco} = \frac{\left(f_{hh} - f_{ll}\right)}{\left(v_{hh} - v_{ll}\right)}, \tag{9}$$

where f_{hh} and f_{ll} denote the highest and lowest frequencies of the VCO, and v_{hh} and v_{ll} are the highest and lowest voltages of the VCO input signal, respectively. If the highest frequency f_{hh} generated by the VCO is assigned for the minimum inductance of the primary winding, then the increase in the position Δl_c will decrease the output frequency of the VCO. The deviation of the frequency Δf can be considered in the form of a voltage signal at the input voltage v_{vco} of the VCO. At the frequency f_{hh}, the input voltage v_{vco} of the VCO is equal to the voltage v_{hh}, which is assigned in the design procedure. The summing amplifier is included in the circuit in Fig. 5(a) as shown in Fig. 5(b). The resistors R_{S1}, R_{S2}, R_{S3}, and R_{S4} in Fig. 5(b) are equal. The capacitance C_S is provided to remove the ripple on the signal v_{vco} without disturbing the operation of the PLL. The voltage signal from the input signal v_{vco} of the VCO is subtracted with the reference voltage V_{ref} to achieve the position signal v_{pos}, where the reference voltage V_{ref} is set to equal the voltage at the VCO input for the position $\Delta l_c = 0$. From the routine circuit analysis, the voltage signal v_{pos} of Fig. 5(b) can be stated as

$$v_{pos} = V_{ref} - \frac{K_f}{K_{vco}} + \frac{K_f K_3}{K_{vco}\left(K_2 + K_3 l_c\right)} \Delta l_c, \tag{10}$$

where K_{vco} is the conversion gain of the VCO in kHz/V. From Eq. (9), the reference voltage V_{ref} is set to equal K_f/K_{vco}. Therefore, Eq. (10) can be rewritten as

$$v_{pos} = \frac{K_f K_3}{K_{vco}\left(K_2 + K_3 l_c\right)} \Delta l_c = \frac{K_f K_c}{K_{vco}} \Delta l_c. \tag{11}$$

Note that the voltage signal v_{pos} is proportional to the change in the position Δl_c. From the inductance characteristic of the primary winding in Fig. 2(c), Eq. (10) can acquire the position Δl_c only a half scale of the LVDT. This is due to the symmetry of the inductance characteristic between the lateral side of the LVDT to the middle and the middle to the other.

The XOR gate X_1 and opamp A_4 shown in Fig. 5(c), where opamp A_4 functions as a comparator, are used to investigate the phase change between the secondary winding signal v_s and the square wave signal v_{sq}. The output signal V_{sign} of the XOR X_1 exhibits a logic "1" for in phase between the signals v_s and v_{sq}. Otherwise, the output signal V_{sign} is "0". The signal V_{sign} is used to indicate the sign of the signal v_{pos}. If the moving core moves in the positive region of the LVDT, then the signal V_{sign} is shown as "0". Also, the signal V_{sign} is "1" if the moving core moves in the negative region of the LVDT. The phase-controlled amplifier (PCA) in Fig. 5(d) is provided to exhibit a full analog signal range v_{fs}, where the resistors R_{S5} to R_{S8} are equal. From Fig. 5(d), opamp A_5 and the resistors R_{S5} to R_{S7} act as a voltage follower for the signal V_{sign} = "0". Also, the signal V_{sign} = "1" causes the phase-controlled amplifier to act as an inverting amplifier with unity gain. The output signal v_{fp} versus the position Δl_c is shown in Fig. 5(e).

3.2 Design procedure

The procedure for designing the TSWG and PLL for the LVDT signal conditioning circuit in this study is as follows.

1. Measure the inductance of the primary winding of the LVDT versus the position of the moving core, where the moving core is varied in the entire full moving range.
2. Set the frequency range of the TSWG, where the maximum and minimum frequencies are determined from the highest and lowest inductances of the primary winding of the LVDT, respectively.
3. Set the frequencies fhh and fll of the PLL equal to the maximum and minimum frequencies of the TSWG, respectively. The conversion gain Kvco of the VCO can then be determined at this procedure.
4. Set the cutoff frequency of the LPF equal to one-tenth of the difference frequency $f_d = (f_{hh} - f_{ll})$ to reduce the ripple in the signal v_{vco}. The resistor R_{lf} and the capacitor C_{lf} can be determined from $R_{lf}C_{lf} = 10/(2\pi f_d)$.

4. Experimental Results

The performance of the proposed technique is confirmed by experimental implementation. The circuit in Fig. 5(a) is implemented using commercial devices such as dual opamps LF353 for opamps A_1 to A_5, PLL CD4046, XOR CD4070, transistor 2N2222A, and zener diode 1N5273 of V_Z = 8.2 V for the zener diodes D_{Z1} and D_{Z2}. Note that CD4046 and CD4070 form the digital CMOS integrated circuit (IC). The resistors $R_1 = R_2$ = 50 kΩ are assigned for a = 1. The resistors R_Z and R_{S1} to R_{S8} are set as 10 and 100 kΩ, respectively. The capacitor C_S is chosen as 1 μF to cancel the ripple of the voltage signal v_{vco}. The power supply voltages of opamps and digital CMOS ICs are ±12 and 12 V, respectively. The upper frequency of the TSWG is assigned as 10 kHz. The LVDT used in this study is a commercial LVDT with a linear range of 2 mm and a structure length of 44.7 mm. The length of the moving core of the LVDT is 31.8 mm. From procedure 1 of Sect. 3.2, the inductance of the primary winding versus the position of the moving core from Δl_c = 0 to ±13 mm is measured as shown in Fig. 6. From Fig. 6, the maximum and minimum inductances of about 438.6 and 267.7 μH, respectively, are observed. Note that the inductance of the primary winding is linearly varied versus the position of Δl_c. The rate of inductance change of about 13.15 μH/mm in Fig. 6 is observed. This inductance is used to determine the resistor R_{tr} from procedure 2. The maximum frequency generated from the TSWG is assigned as 50 kHz. From Eq. (4), the resistor R_{tr} can be determined as 57.46 Ω. The variable resistor of 100 Ω is used instead of the resistor R_{tr} to fine-tune its resistance for the TSWG to generate the desired frequency. The minimum frequency generated from the TSWG can be determined as 29.84 kHz. The experimental setup of the proposed technique is shown in Fig. 7. The conversion gain K_{vco} of the VCO can be measured as 8.33 kHz/V. The measured frequency of the TSWG versus the position Δl_c of the LVDT is shown in Fig. 8. From procedure 3, the frequencies f_{hh} and f_{ll} of the PLL are set to equal the maximum and minimum frequencies of the TSWG, respectively. The capacitor C_f and the resistors R_{f1} and R_{f2} can be determined from the

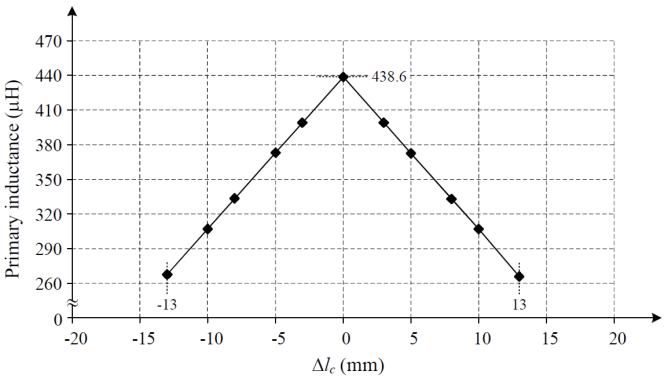


Fig. 6. Measured inductance of primary winding.

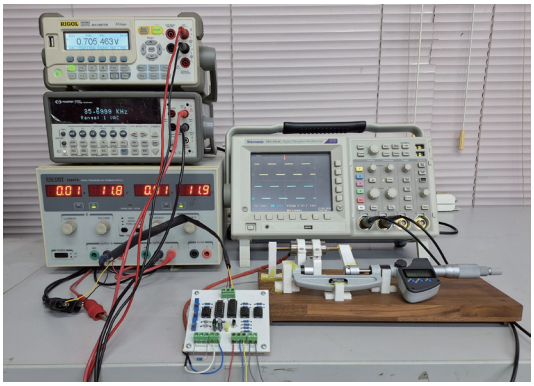


Fig. 7. (Color online) Experimental setup.

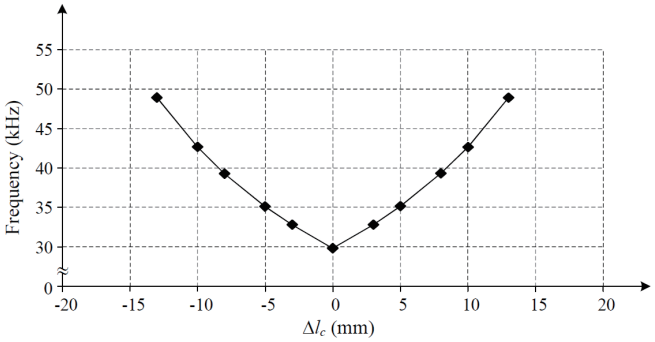


Fig. 8. Measured output frequency of TSWG.

PLL CD4046 specification as C_f = 0.01 μF, R_{f1} = 1.5 kΩ, and R_{f2} = 200 kΩ. The variable resistors of 2 and 500 kΩ are used to replace the resistors R_{f1} and R_{f2}, respectively, for tuning the desired frequency. Also, the resistor R_{lf} can be determined as 7.95 kΩ for C_{lf} = 0.01 μF. From the circuit in Fig. 5(a), the voltage signal v_{vco} is measured for the moving core varied in full range as

shown in Fig. 9. It can be seen that the voltage signal v_{vco} exhibits the piecewise linear behavior. The maximum inductance of the primary winding causes the TSWG and PLL to generate the lowest frequency of about 29.84 kHz. At this frequency, the input voltage v_{vco} of the VCO is measured as 4.5 V, which is called the offset voltage V_{off}. The reference voltage V_{ref} is set to equal the offset voltage V_{off}. If the circuits in Figs. 5(b)–5(d) are applied to the circuit in Fig. 5(a), then the voltage signal v_{pos} for the full stroke range of the LVDT is obtained. Figure 10(a) shows the measured voltage v_{pos} from the output of the PCA. Note that the conversion gain of the proposed circuit is 0.1764 V/mm. The percentage error of the measured value in Fig. 10(a) is

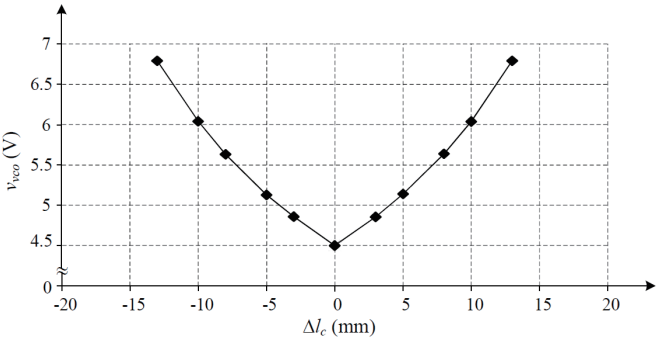
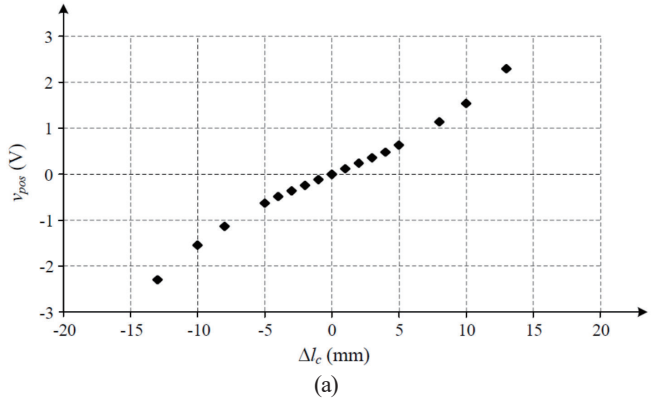
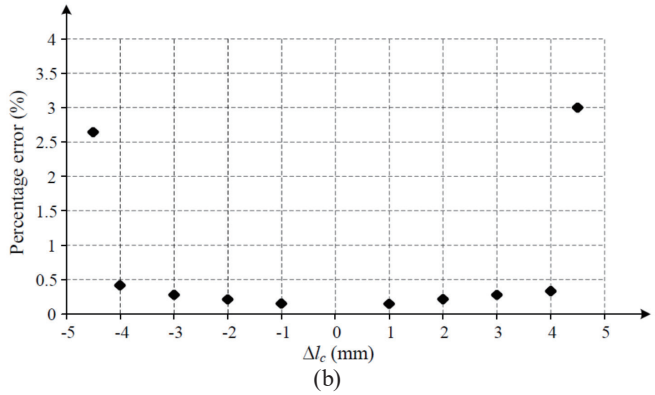


Fig. 9. Measured voltage signal v_{vco} versus position Δl_c.



(a)



(b)

Fig. 10. (a) Measured voltage v_{pos} and (b) percentage error.

shown in Fig. 10(b). From Fig. 10(b), if the maximum percentage error of 0.5% is the same as the specific error of the LVDT used in this study, then the position Δl_c can be varied over ±4 mm. It can be seen that the proposed technique can extend the operating range of the LVDT more than twofold.

5. Conclusions

The LVDT signal conditioning circuit has been proposed in this paper. The operation of the LVDT used in the proposed technique is based on self-oscillation. Therefore, the proposed technique does not require an external oscillator for the LVDT. The position extraction is based on the use of the PLL principle. The linear operating range can be extended more than twofold without disturbing the LVDT structure. The performance of the proposed technique is confirmed by experimental implementation. The results demonstrating the performance of the proposed technique are theoretically expected. All the components used in the proposed circuit are commercially available. The configuration of the proposed circuit is simple and inexpensive, which is suitable for embedded measurement in small or micro robots.

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