

# 38 GHz All-pass Phase Shifter with Attenuator Using 0.15 $\mu\text{m}$ GaAs Technology for Wireless Sensors

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A 38 GHz all-pass phase shifter designed using the pHEMT 0.15  $\mu\text{m}$  GaAs process is presented. The phase shifter consists of two groups of a low-pass filter (LPF) with a  $90^\circ$  phase shift and attenuators. By tuning the bias voltage, the magnitude and phase of the signal are changed. At the end of the circuit, a power combiner is used to obtain a  $360^\circ$  all-pass output signal. The measurement results show that the phase shifter can achieve phase variation with an insertion loss of about 10 dB and an all-pass work function around a center frequency of 38 GHz. The chip area is about  $1.12 \text{ mm}^2$ . The phase shifter is suitable for sensing circuitry.

## 1. Introduction

The application of next-generation wireless communication systems requires high-speed data transport. A phase array beaming system was first proposed in the early 1900s and has experienced tremendous development over the past decades.<sup>(1)</sup> Recent research has proved the importance of wireless sensors for beaming systems.<sup>(2)</sup> A phase shifter is a vital element in a phase array system and is also used in sensors for phase detection.<sup>(3)</sup> The all-pass phase shifter has the greatest freedom because it can offer a full  $360^\circ$  output. Early all-pass phase shifters used a combination of two  $180^\circ$  varactor linear phase shifters.<sup>(4)</sup> Other broadband all-pass phase shifters<sup>(5,6)</sup> were proposed with hybrid or cascading structures. However, they are too large for modern integration. A hybrid analog and digital phase shifter<sup>(7)</sup> was devised as a way of all-pass realization, but the resolution was not continuous. A way of realizing continuous tuning is to use voltage-controlled methods through a vector sum,<sup>(8,9)</sup> and the phase can be tuned linearly with an infinite resolution via the control voltage. The resolution of a digital phase shifter is limited.<sup>(10)</sup> Analog phase shifters are continuous but have a relatively high insertion loss or a large area. The idea of using a vector sum method for an all-pass phase shifter was presented for voltage gain amplifiers.<sup>(11)</sup> However, some power consumption is still required.

An all-pass phase shifter using a vector sum method with an attenuator can solve the defects of the past phase shifters. It can achieve zero power consumption. In this paper, a 38 GHz all-pass phase shifter is demonstrated using voltage-controlled, switch-type, and vector sum

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techniques in a 0.15  $\mu\text{m}$  GaAs process. This hybrid all-pass phase shifter achieves full  $360^\circ$  operation with a low insertion loss, a small size, and an infinite resolution. This work can help to improve the tolerance and practical performance of phase shifters used in sensors.

## 2. Circuit Design and Implementation

The proposed 38 GHz all-pass phase shifter is shown in Fig. 1. The first stage is a coupler, which divides the input signal into two signals of  $180^\circ$  phase difference. The second stage consists of two low-pass filters (LPFs). The LPFs are tuned by the bias voltage, and the output signal phase can be changed by  $90^\circ$  by a suitable bias voltage. The third stage comprises two attenuators for tuning the magnitude of the signals, which are also controlled by the bias voltage. The two channel signals are combined by a power combiner, and a  $360^\circ$  phase signal is finally generated.

For the combination of the two signals before the power combiner, the output signal is expressed as follows.

$$I_{\theta_{out}} = I_{\theta_1} + I_{\theta_2} \quad (1)$$

$$I_{\theta_1} = a \sin \omega t \quad (2)$$

$$I_{\theta_2} = b \cos \omega t \quad (3)$$

$$I_{\theta_{out}} = \sqrt{a^2 + b^2} \sin \left( \omega t + \tan^{-1} \frac{b}{a} \right) \quad (4)$$

Here,  $I_{\theta_1}$  and  $I_{\theta_2}$  represent signals in paths A3 and B3, and  $a$  and  $b$  are the magnitudes of signals A3 and B3 shown in Fig. 1, respectively. The output signal phase achieves a continuous  $360^\circ$  variation by tuning the phases of the two channel signals.

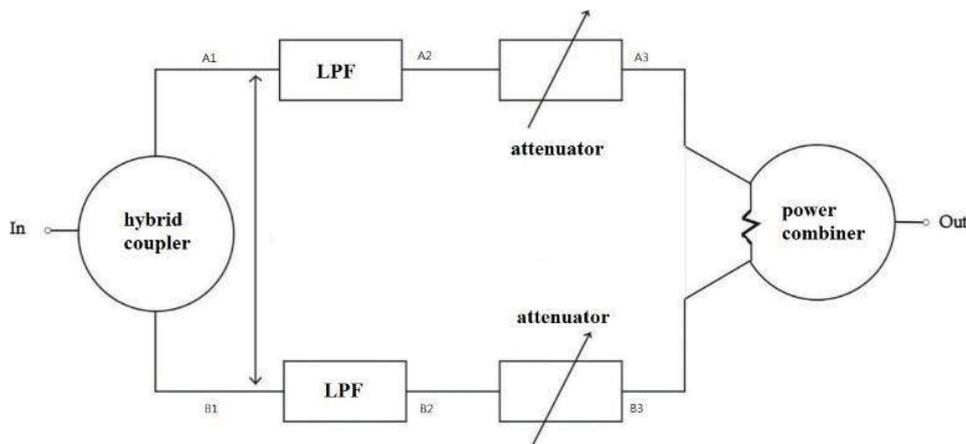


Fig. 1. Block diagram of the phase shifter.

The phase of each signal is shown in Fig. 2. At the beginning, the input signal is divided into signals A1 and B1, which have a phase difference of 180°, and the insertion loss is about 3 dB. An LPF is designed with a tunable function of a 90° phase shift. The bias voltage of the LPF is 0–2 V and the insertion loss is about 4 dB. The attenuator operates the previous amplitude signals (A2, B2). The amplitude of the signal can be tuned by the bias voltage. Hence, for the maximum and minimum bias voltage conditions, we can ideally assume that the signal is fully passed or blocked. After the attenuator, signals A3 and B3 are combined by the power combiner. The insertion loss of the power combiner is about 3 dB at 38 GHz. The Agilent design system was used to calculate the S-parameters of each component and to optimize the geometry of the phase shifter to reduce the insertion and return losses.

The hybrid coupler is composed of a pair of LC series circuits as shown in Fig. 3. It separates the input signal into two sets of signals with a phase difference of 180°. The LPF

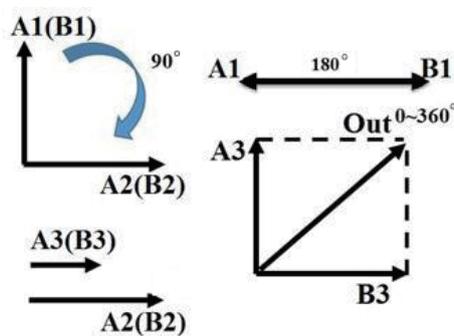


Fig. 2. (Color online) Phase states of all stages.

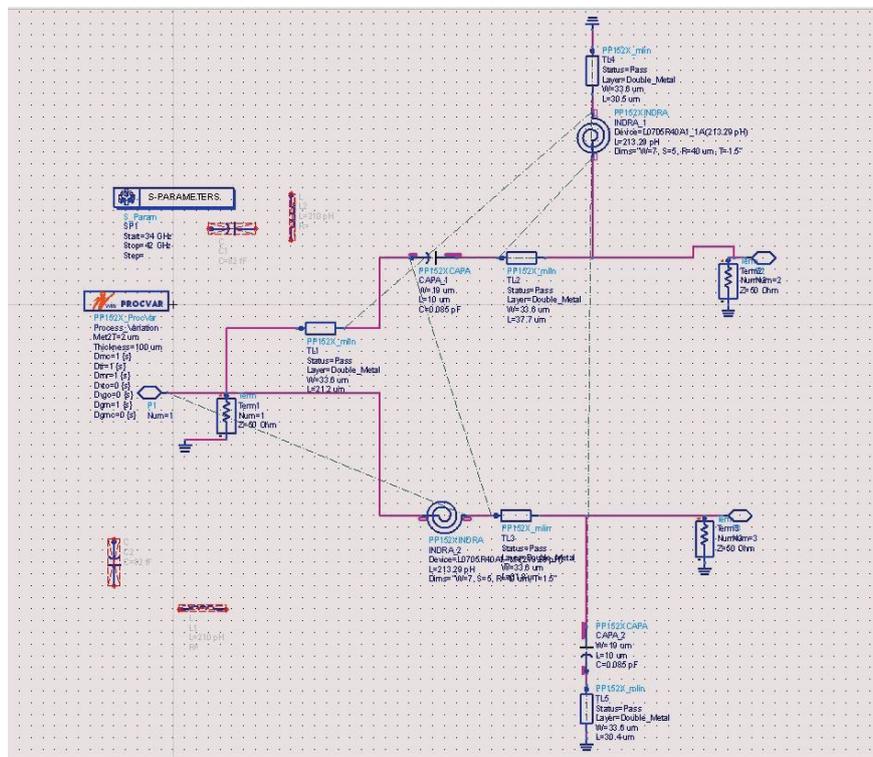


Fig. 3. (Color online) Schematic of the hybrid coupler.

consists of three inductors, three capacitors, one resistor, and four diodes as shown in Fig. 4. It can filter out high-frequency signals and produce a  $90^\circ$  phase difference via voltage control. Figure 5 shows the attenuator. Its function is to control the signal intensity. Figure 6 shows the schematic of the power combiner located at the last stage of the phase shifter. The phase shifter was implemented by a  $0.15\ \mu\text{m}$  pHEMT GaAs process, and a microphotograph of the chip is shown in Fig. 7. At a tuning voltage of  $0\text{--}10\ \text{V}$ , the simulated insertion loss varies linearly from  $1.5$  to  $22.1\ \text{dB}$  as shown in Fig. 8. The chip dimensions are as small as  $1.6 \times 0.7\ \text{mm}^2$ . The signals

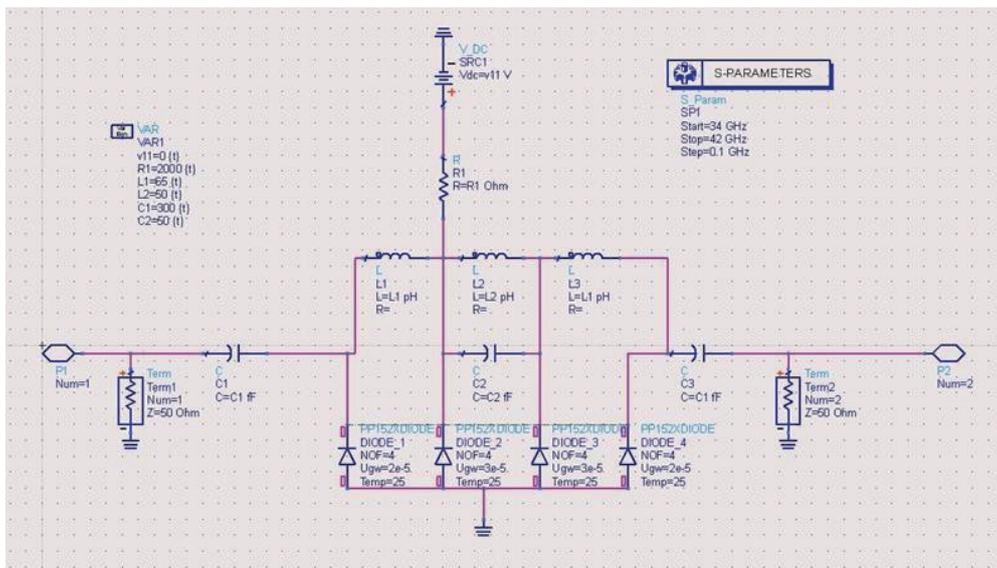


Fig. 4. (Color online) Schematic of the LPF.

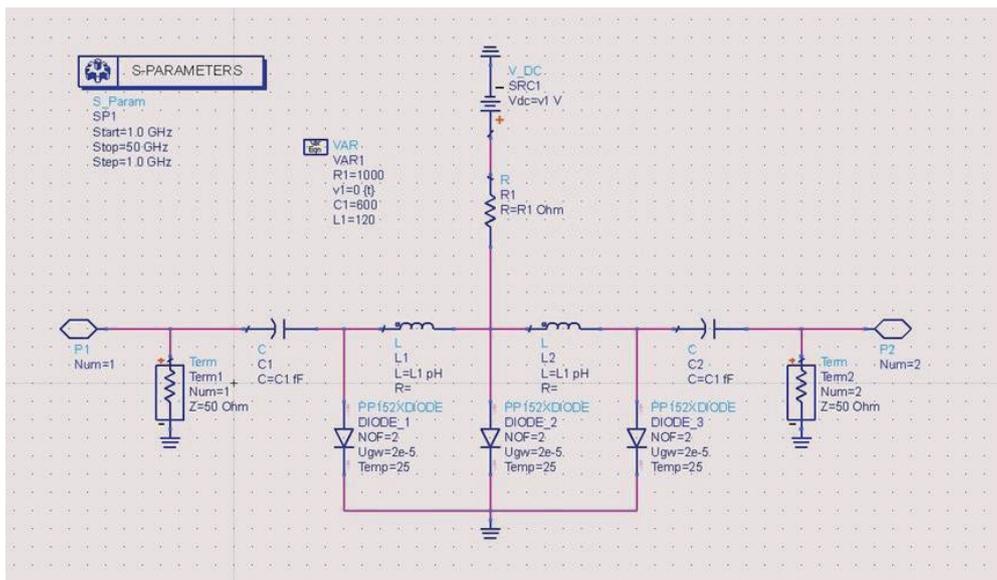


Fig. 5. (Color online) Schematic of the attenuator.

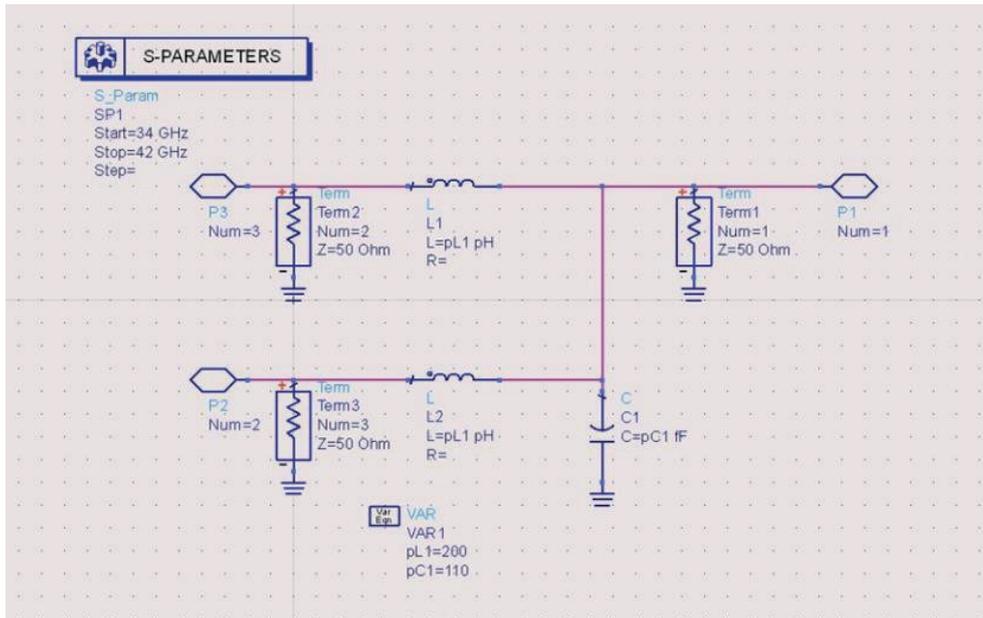


Fig. 6. (Color online) Schematic of the power combiner.

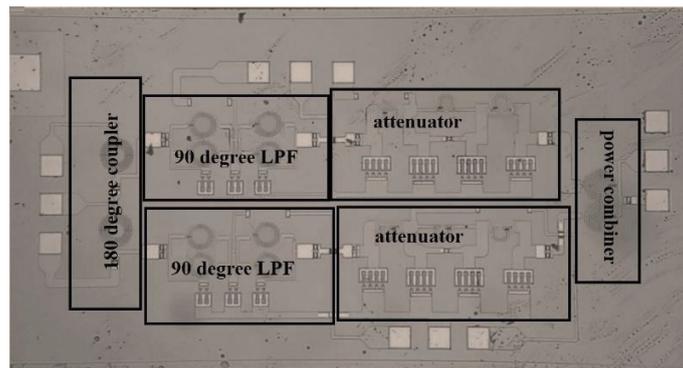


Fig. 7. (Color online) Photograph of the fabricated chip.

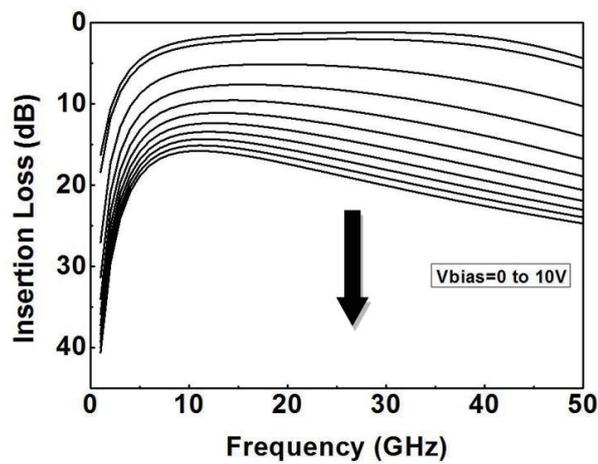


Fig. 8. Simulated insertion loss of the attenuator as the bias voltage is varied from 0 to 10 V.

were measured on-wafer using an Agilent E8361A network analyzer. The losses of the probes and cables were calibrated separately.

### 3. Results and Discussion

Figure 9 shows the measured and simulated return and insertion losses of the proposed phase shifter as functions of the frequency within the range of 34–42 GHz. The average of the simulated and measured results is swept by different bias voltages. The insertion loss is about 10 dB and the return loss is above 13 dB at a frequency of 38 GHz, and the measured results are in good agreement with the simulated results.

The error between the ideal and simulated results is due to the ideality assumption of the attenuators, and the error between the simulated and measured results is caused by the parasitic elements of the circuits. The measured results in Fig. 10 also show that by tuning the bias voltages, the phase shifter can also achieve a full 360° output.

A comparison of the performance of the proposed phase shifter with those of the other reported phase shifters is shown in Table 1. The proposed phase shifter can provide good insertion and return losses with a continuous output tuning range of 360°.

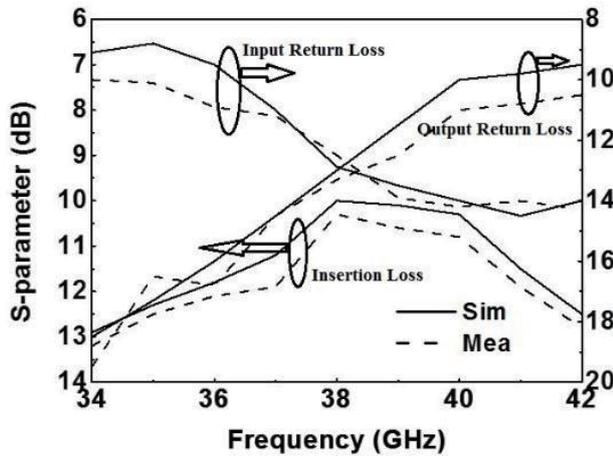


Fig. 9. Measured and simulated insertion and return losses of the phase shifter as functions of frequency.

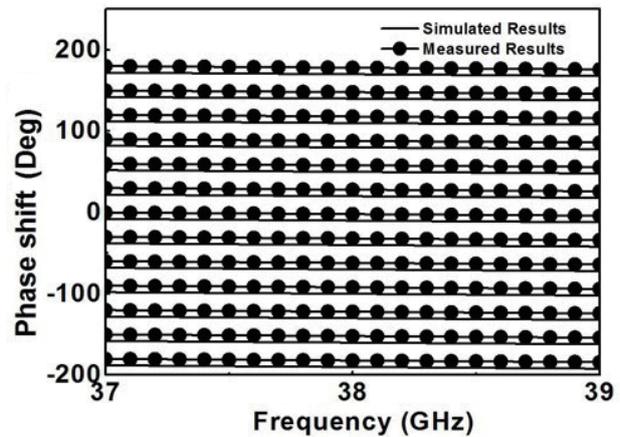


Fig. 10. Measured output signal phases at different bias voltages.

Table 1  
Comparison of proposed phase shifters.

Reference	Technology	Frequency (GHz)	Working function	Insertion loss (dB)	Return loss (dB)	Size (mm <sup>2</sup> )
5	GaAs	2–18	360/hybrid continuous	10	9	192
6	GaAs	16–18	Continuous	4.2 ± 0.9	N/A	7.44
7	0.13 μm CMOS	22–26	Hybrid	1.5	N/A	1.42
9	0.18 μm CMOS	22–26	360/continuous	15.3	16	0.31
10	0.15 μm GaAs	60	30 bit	7.5–10.7	N/A	3
This work	0.15 μm GaAs	38	360/continuous	10	13	1.12

## 4. Conclusions

An all-pass 38 GHz phase shifter implemented by the 0.15  $\mu\text{m}$  GaAs pHEMT process has been presented. Voltage-controlled and switch-type techniques are utilized to achieve a continuous tuning range. Moreover, owing to the use of two-channel hybrid signals with the vector sum principle, the circuit obtains a full 360° output. The measured phase error is due to the parasitic elements. The results show that the circuit exhibits good insertion and return losses and a small chip size without sacrificing the performance of phase error. It is suitable for phase array and multiantenna beamforming systems and sensor applications.

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